Simultaneous Multithreading Support in Embedded Distributed Memory MPSoCs

Rafael Garibotti, Luciano Ost, Rémi Busseuil, Mamady Kourouma,
Chris Adeniyi-Jones, Gilles Sassatelli, Michel Robert
{garibotti, ost, busseuil, kourouma, sassatelli, robert}@lirmm.fr
Chris.Adeniyi@arm.com

1. Contributions

- Improved programmability through POSIX-like threads API in a distributed memory MPSoC
- Remote Memory Access (RMA) and memory consistency support, allowing vSMP clusters definition at run-time
- Improved performance scalability
- Mechanisms validated in a synthesizable RTL NoC-based MPSoC

2. Multithreading Platform

- Native message passing
- Remote Memory Access (RMA) and memory consistency support, allowing vSMP clusters definition at run-time
- Improved performance scalability

3. Experimental setup and Results

- Reference Platforms (reproduced with GEM5 Simulator):
  - Up to 8 ARM Cortex-A9 (500MHz), Linux Kernel 2.6.38
  - 16kB private L1 data and instruction caches
  - 32bits channel width
  - 256MB unified L2 data and instruction caches
  - DDR physical memory running at 400MHz
- Adopted Platform:
  - NoC 3x3, handshake, 500MHz clock frequency
  - 4 input buffer positions
  - Cache size 4kB / 8kB / 16kB (8 words per lines)

- PE area evaluated at 40nm CMOS Technology

<table>
<thead>
<tr>
<th>Memory Size</th>
<th>Low-Power core with FP</th>
<th>Low-Power core with FP + RMA</th>
<th>Area Overhead</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 kB</td>
<td>0.2803 mm²</td>
<td>0.3240 mm²</td>
<td>15.59%</td>
</tr>
<tr>
<td>128 kB</td>
<td>0.4392 mm²</td>
<td>0.4829 mm²</td>
<td>9.94%</td>
</tr>
<tr>
<td>256 kB</td>
<td>0.7650 mm²</td>
<td>0.8088 mm²</td>
<td>5.72%</td>
</tr>
</tbody>
</table>

Multi-applications scenario

Mapping configuration

Each bar represents the execution time of one worker thread

Performance overhead related to the host placement

<table>
<thead>
<tr>
<th>Cache Size</th>
<th>Currory</th>
<th>Center (11)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 kB</td>
<td>100%</td>
<td>90.51%</td>
</tr>
<tr>
<td>8 kB</td>
<td>100%</td>
<td>96.84%</td>
</tr>
<tr>
<td>16 kB</td>
<td>100%</td>
<td>96.90%</td>
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