

Mont-Blanc 2020 Project Looks to Pave the Way for New European Exascale Processors

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LES CLAYES, France, Dec. 15, 2017 — Following on from the three successive Mont-Blanc projects since 2011, the three core partners Arm, Barcelona Supercomputing Center and Bull (Atos Group) have united again to trigger the development of the next generation of industrial processor for Big Data and High Performance Computing. The Mont-Blanc 2020 consortium also includes CEA, Forschungszentrum Jülich, Kalray, and SemiDynamics.

The Mont-Blanc 2020 project has a budget of 10.1 million Euros, funded by the European Commission under the Horizon2020 program. It was launched on 11th December at the Atos site in Les Clayes (France), with a kick-off meeting that gathered representatives of all partners.

The Mont-Blanc 2020 project intends to pave the way to the future low-power European processor for Exascale. To improve the economic sustainability of the processor generations that will result from the Mont-Blanc 2020 effort, the project includes the analysis of the requirements of other markets. The project's strategy based on modular packaging would make it possible to create a family of SoCs targeting different markets, such as "embedded HPC" for autonomous driving. The project's actual objectives are to:

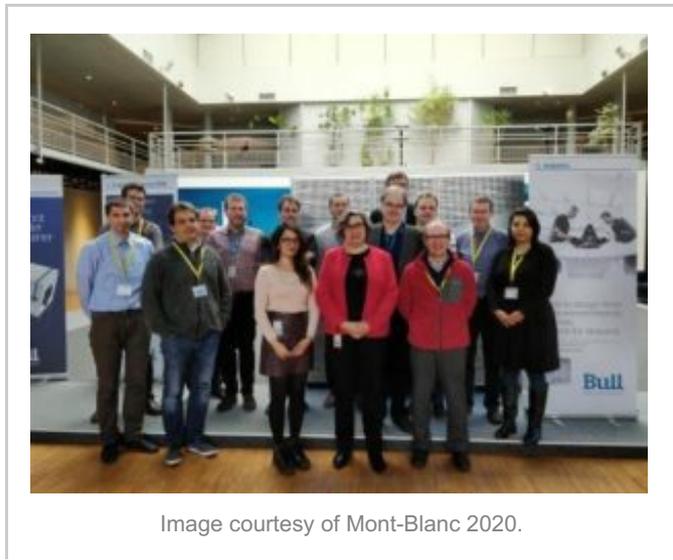


Image courtesy of Mont-Blanc 2020.

- define a low-power System-on-Chip architecture targeting Exascale;
- implement new critical building blocks (IPs) and provide a blueprint for its first

- generation implementation;
- deliver initial proof-of-concept demonstration of its critical components on real life applications;
- explore the reuse of the building blocks to serve other markets than HPC, with methodologies enabling a better time-predictability, especially for mixed-critical applications where guaranteed execution & response times are crucial.

The project will have to tackle three key challenges to achieve the desired performance with the targeted power consumption:

1. understand the trade-offs between vector length, NoC bandwidth and memory bandwidth to maximize processing unit efficiency;
2. an innovative on-die interconnect that can deliver enough bandwidth to the processing units, with minimum energy consumption;
3. a high-bandwidth and low power memory solution with enough capacity and bandwidth for Exascale applications.

“The ambition of the consortium is to quickly industrialize our research. This is why we decided to rely on the Arm instruction set architecture (ISA), which is backed by a strong software ecosystem. By leveraging the current efforts, including the Mont-Blanc ecosystem and other international projects, we will benefit from the system software and applications required for successful usage” explained Said Derradji, Atos, coordinator of the Mont-Blanc 2020 project.

About the Mont-Blanc 2020 project

Mont-Blanc 2020’s goal is to initiate a family of processors that will be the basis for European Big Data / High Performance Computing exascale systems, and that will achieve market adoption and economic sustainability.

The Mont-Blanc 2020 project is run by a European consortium that includes: Atos / Bull, the European number one in Big Data and High Performance Computing (coordinator, France);

- Arm, the world’s leading semiconductor IP company (United Kingdom);
- Barcelona Supercomputing Centre, the national supercomputing centre in Spain;
- CEA, the French Alternative Energies and Atomic Energy Commission;
- Forschungszentrum Jülich, one of the largest interdisciplinary research institutions in Europe (Germany);
- Kalray, a leading innovator with its supercomputing on a chip MPPA solutions (France);
- SemiDynamics, a specialist in microprocessor architecture, front-end design and verification services (Spain).

This project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 779877.

Source: Mont-Blanc 2020

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