HPC NEWS

Mont-Blanc project sets exascale aims

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Energy efficiency is already a primary concern for the design of any computer system and it is recognised that future Exascale systems will be strongly constrained by their power consumption. This is why the Mont-Blanc project, which was launched on 14 October in Barcelona with a kick-off meeting, has set itself the following objective: to design a new type of computer architecture capable of setting future global HPC standards that will deliver Exascale performance while using 15 to 30 times less energy.

This new project, coordinated by the Barcelona Supercomputing Center (BSC) and with a budget of more than 14 million Euros, including more than 8 million Euros funded by the European Commission, has three objectives:

• to develop a fully functional energy-efficient HPC prototype using low-power commercially available embedded technology;

• to design a next-generation HPC system together with a range of embedded technologies in order to overcome the limitations identified in the prototype system; and

• to develop a portfolio of Exascale applications to be run on this new generation of HPC systems.

With energy efficiency being a key issue, supercomputers are expected to achieve 200 Petaflop/s (PF) in 2017 with a power budget of 10 MW, and 1000 PF (1 Exaflops/s) in 2020 with a power budget of 20MW. That means an increase in energy-efficiency of more than 20 times compared with the most efficient supercomputers today.

Alex Ramirez, leader of the Mont-Blanc project, said: 'First, we must take into account that not all energy is used for computing within the cores. In current systems the processors consume the lion's share of the energy, often 40 per cent or more. The remaining energy is used to power up the memory, interconnection network, and storage system. Furthermore, a significant fraction is wasted in power supply overheads, and in thermal dissipation (cooling), which do not contribute to performance at all.'

The system architecture in Mont-Blanc will rely on energy-efficient ARM processors, also used in embedded and mobile devices. It is expected to achieve from 4 to 10 times increase in energy-efficiency compared with current technologies.

The Mont-Blanc project brings together a purely European consortium which joins industrial technology providers and research supercomputing centres: Bull, as the major HPC system vendor, ARM, as the world leader in embedded high-performance processors, and Gnodal, as interconnect partner that focuses its new product on scalability and power efficiency. Besides the technology providers, Mont-Blanc unites the supercomputing centres from the four Tier-0 hosting partners in PRACE who have leading roles in system software and Exascale application development: Germany (Forschungszentrum Jülich, BADW-LRZ), France (GENCI, CNRS), Italy (CINECA), and Spain (BSC).

They also run thousands of real applications on a daily basis on their Tier-0 and Tier-1 systems, coming from a vast number of scientific domains and serving a large community of academic and industrial users. In order to assess the different hardware and software components made available

during the project, an incremental approach will be used, working on both the porting and the optimisation of small kernels, and then on real end-users scientific applications.

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