Mont-Blanc 2020: Simulation Efforts Towards Exascale High Performance Computing

Embedded Tutorial on "DDECS-2020"

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***Abstract*—The Mont-Blanc project follows a co-design approach to ensure the final hardware design meets real-world High-Performance Computing (HPC) application requirements. Simulation is widely used in system design for evaluating different design options, as well as to characterize how an application will run in that configuration. The main idea is to test the applications and evaluate future performance prior to silicon availability. One of the most widely used simulation tools in research and in the Mont-Blanc series project is the gem5 simulator. gem5 is an open source, modular platform for computer-system architecture that is flexible and highly configurable. It can model a whole system architecture as it includes different models for the cores and the memory hierarchy. The objective of this tutorial, is to present in a our simulation framework, and how it has help on the design of highly complex systems.**

***Index Terms*—ARM, HPC, Co-design, gem5, Mont-Blanc 2020.**

I. Introduction

Simulation is widely used in system design for evaluating different design options. Depending on the abstraction level considered for simulating a given system configuration, there is a trade-off between the obtained precision and speed. Generally, simulating a detailed system model provides accurate evaluation results at the price of potentially high simulation time. On the other hand, less detailed or more abstract system representations usually provide less accurate evaluation results, but in a fast and cost-less manner. In practice, such representations are defined such that they only capture system features that are most relevant to the problem addressed by a designer. In order to take the correct decisions while designing given system configuration, we need simulation tools that targets different trade-offs between accuracy and simulation speed.

II. Tutorial Structure

In the first part of the tutorial we will present the Mont-Blanc 2020 project. We will present the project consortium and the interaction between academy and industrial research, while providing details on how our project will help on the development of the first European Processor for High-Performance Computing applications. Moreover, we will introduce our Multi-Scale Simulation Framework, developed under the Mont-Blanc 3 and used in the Mont-Blanc 2020 project (Fig. 1).

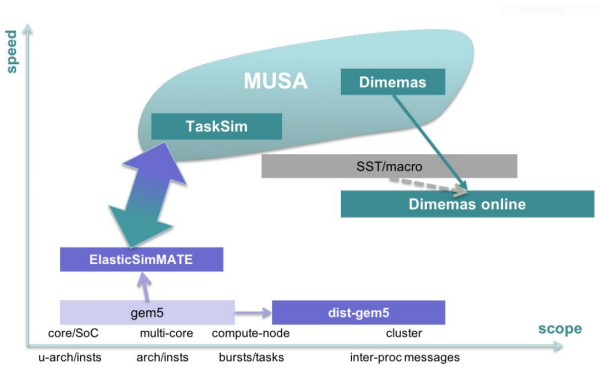

Fig. 1. Multi-Scale Simulation Framework.

In the second part of the tutorial, we will focus our attention to one of the main tools used in our framework. We will introduce the the gem5 simulator [1]. gem5 is an open source, modular platform for computer-system architecture that is flexible and highly configurable. It can model a whole system architecture as it includes different models for the cores and the memory hierarchy. We will show the participant of the tutorial, how to compile and run a "Hello World" case on an Homogeneous and a Heterogeneous (big.LITTLE) Arm system [2].

In the third part of the tutorial, we will present the use of trace-driven simulation for simulation performance and scalability analysis. This simulation approach targets a reduction on the simulation time while keeping high accuracy levels. In this part, we will show simulation results of the ElasticSimMATE approach, and explain how it can be used to perform strong/weak scaling analysis, along side with architectural parameter exploration [3]

In the last part of the tutorial, we will present the Mont-Blanc 2020 extensions of gem5. Mont-Blanc 2020 has been instrumental on the implementation of the Scalable Vector Extension in gem5 [4], [5]. The particular release produced as part of Mont-Blanc 2020 [6] adds support for the Arm Scalable Vector Extension (SVE) ISA extension. SVE provides advanced vector instructions that decouple the width of the hardware vector registers and computation units from the ISA level. The same application binary will work with hardware vector widths ranging from 128 bits to 2048 bits. This is particularly interesting, from the point of view that SVE real hardware is not yet available, but performance evaluation can start based on our proposed extensions. Finally, as power consumption is a key factor on the design of any system, we will also present the proposed on-line power modeling capability for SVE architectural systems.

In summary, tutorial participants will become familiar with how the simulation infrastructue of the Mont-Blanc project series and more specifically on how the different uses of the gem5 simulator, its use for HPC system exploration, and the recent capabilities that allows simulation of ARM sve systems

III. Intended Audience

The Mont-Blanc project is a collaborative project between academia and industry. We strongly believe this tutorial will be of interest for professionals that first want to know more about how a European project works and second on how that work is reflected in terms of tools and research capabilities. Moreover, it would be attractive for people working on the area of System-on-Chip and Network on Chip design as well as HW/SW interaction, and how they can use it to assess and solve own HPC problems.

Acknowledgment

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Speaker Biography

Alejandro NOCUA received the Ph.D. degree in Microelectronics from the University of Montpellier, France, in 2016. Currently, he is an R&D Engineer in SoC ARM Modeling at BULL Atos technology, he is collaborating in the Mont-Blanc 2020 and EPI projects developing models for early software development. His research interests include the analysis of high-performance computing and energy-efficiency design methodologies. Before he was a postdoctoral researcher at the French National Center for Scientific Research (CNRS) and works in the Microelectroncis Deparment of the LIRMM Laboratory of Informatics, Robotics and Microelectronics of Montpellier. He received his Master degree in Science from the National Institute of Astrophysics, Optics and Electronics (INAOE), Mexico, in 2013. Alejandro was awarded BS degree in Electronics Engineering from Industrial University of Santander (UIS), Colombia in 2011.